International Journal of Recent Engineering Research and Development (IJRERD)
ISSN: 2455-8761
www.ijrerd.com || Volume 06 – Issue 12 || December 2021 || PP. 23-31

Design and Analysis of Two Stage and Single Stage OP-AMP in 90nm CMOS Technology

Pham Duy Khanh[1], Tran Van Binh[2], Nguyen Thi Xoan[3], Ha Ngoc Thuan[4]
[1,2,3,4]*Faculty of Electronic Engineering, Thai nguyen University of Technology,*
666, 3/2 street, Tich Luong ward, Thai Nguyen, Viet Nam

Abstract: Today, CMOS technology has played a large role in the development of high-density and low-power VLSI circuits. Two-stage Op-Amps are commonly employed in linear and nonlinear circuits. This paper presents the design and analysis of a two-stage and single stage Op-Amp using 90nm process CMOS technology. In this design, we use 1.8V power supply, 20µA bias current, ratio W/L, slew rate 25V/µs and keep the value of input common-mode ratio constant. In addition, authors show a comparision of the two-stage and single-stage Op-Amp design parameters with requirements. From there, the benefits of two-stage op-amp are going to be shown. The design diagram, simulation results, and layout of the proposed design have been done on Cadence software.

Keywords: Op-Amp; CMOS Analog circuit; buffered Op-Amp; single state CMOS Op-Amp; two-stage CMOS Operational Amplifier; 90nm technology; Cadence

1. Introduction

The operational amplifier is a flexible device and plays a very important role in analog circuit design. It is one of the basic building blocks of linear and nonlinear circuits design. When feedback is applied, the closed-loop transfer function of op-amp is practically independent of gain because operational amplifiers have enough high gain [1],[2],[4],[6],[8]. When we need higher gains, we can use two or more amplifier stages in structure op-amp. There are many op-amp topologies, such as single state, two stage, folded cascode, telescopic but two stage op-amp is popular and widely used. A big part of overall gain in op-amp is provided by the differential-input stage, which improves noise and offset performance [9],[10]. If a low-resistance load is connected with op-amp, a buffer stage is needed after the second stage to keep lower the output resistance and large swing. Using bias circuits to work out suitable operating point for each transistor in its quiescent mode. To get stable closed-loop performance, we need to compensative circuit in the design.

2. Design procedure

In this paper, we proposed two stage and single state Op-Amp with required performance and technology specifications of the amplifier in Table 1.

Table 1. Required specifications for designing two statge and single stage Op-Amp

Specifications parameter	Value in 90nm technology
Technology	90nm
Load Cap (C_L)	2pF
Gain	>50 dB
Phase Margin	$>60^o$
Bandwith (GB)	30 MHz
Slew Rate(SR)	25 V/µs
ICMR(+)	1.6
ICMR(-)	0.8
Power	<=300µW

2.1 Design of two stage Op-Amp

General block diagram of two stage Op-amp is shown in Figure 1 [2],[3],[7].

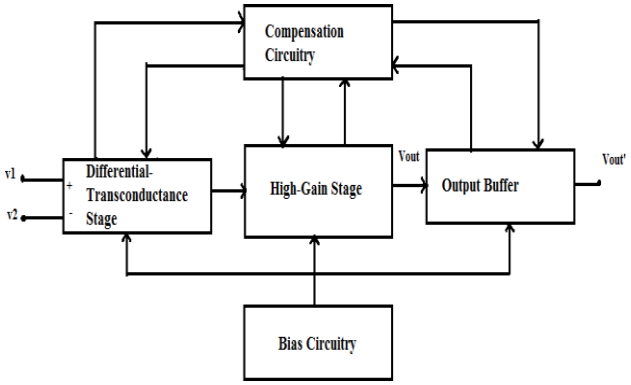

Figure 1. General block diagram of two stage Op-Amp

Table 2 includes the specification parameters given by the designer for the 90nm technology.

In this study, we used two stage Op-Amp topology as show in Figure 2 with required device parameters illustrated in Table 2.

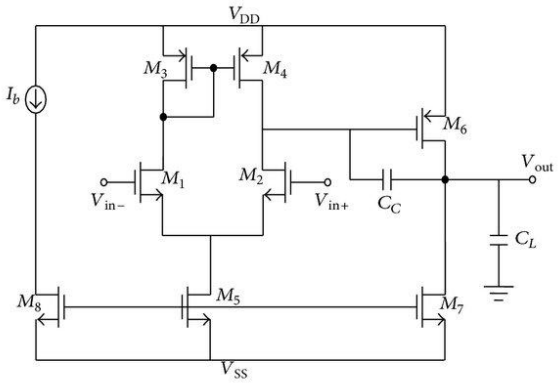

Figure 2. Topology of two stage Op-Amp

Table 2. Required device parameters for designing two statge Op-Amp

Model or device parameters	Value
$\mu_n C_{ox}$	190 μA/V^2
$\mu_p C_{ox}$	87.6 μA/V^2
V_{Dsat}	0.336 V
V_{t3max}	0.187 V
V_{t1min}	0.26 V

In this design, we use some important relationships describing performance of an Op-Amp[1], [2], [6].

- Slew rate: $SR = \frac{I_5}{C_C}$ (1)
- First-stage gain

$$A_{v1} = -\frac{g_{m1}}{g_{ds2} + g_{ds4}} \quad (2)$$

- Second-stage gain

$$A_{V\mathbf{2}} = -\frac{g_{m\mathbf{6}}}{g_{ds\mathbf{6}} + g_{ds\mathbf{7}}} \tag{3}$$

- Gain bandwidth, $GB = \frac{g_{m\mathbf{1}}}{C_C}$ (4)

$$ICMR(+) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - [V_{T3\max}] + V_{T1\min} \tag{5}$$

$$ICMR(-) = V_{SS} + \sqrt{\frac{I_3}{\beta_1}} + V_{T1\max} + V_{DS5sat} \tag{6}$$

To design the circuit, we proceed with the following steps:

Step 1: Find C_c
From the desired phase requirement, we can choose the minimum value for the capacitor C_C according to the following formula:

$$C_C \geq \mathbf{0.4}C_L \tag{7}$$

with C_L = 2pF $\Rightarrow C_C \geq \mathbf{0.8\,pF}$
We choose C_C = 800 pF.

Step 2: Design for transistor M1 and M2 to achieve desired GB
We have :

$$\left(\frac{W}{L}\right)_{\mathbf{1,2}} = \frac{g_{m\mathbf{1}}^{\mathbf{2}}}{\mu_n C_{ox}.\mathbf{2}I_D} \tag{8}$$

With:
$$g_{m\mathbf{1}} = GB.\mathbf{C}_C.\mathbf{2}\pi = \mathbf{30}MHz.\mathbf{800}\,pF.\mathbf{2}\pi$$
$$\Rightarrow g_{m\mathbf{1}} = \mathbf{160}\mu A/V$$
$$\Rightarrow \left(\frac{W}{L}\right)_{\mathbf{1,2}} = \mathbf{6.7}$$

Choose L = 500 nm $\rightarrow$ W = 3 μm.

Step 3: Design for M3 and M4 from the maximum input voltage [ICMR(+)] specification

$$\left(\frac{W}{L}\right)_{\mathbf{3,4}} = \frac{\mathbf{2}I_{\mathbf{3}}}{\mu_p C_{ox}(V_{\mathbf{DD}} - ICMR_+ - V_{t_{\mathbf{3max}}} + V_{t_{\mathbf{1min}}})^{\mathbf{2}}} \tag{9}$$

With:

$$\begin{cases} V_{\mathbf{DD}} = \mathbf{1.8}V \\ ICMR_+ = \mathbf{1.6}V \\ V_{t_{\mathbf{3max}}} = \mathbf{0.187}V \\ V_{t_{\mathbf{1}_{min}}} = \mathbf{0.26}V \\ I_{\mathbf{3}} = \mathbf{10}\mu A \\ \mu_p C_{ox} = \mathbf{87.6}\mu A/V^{\mathbf{2}} \end{cases}$$

Substituting the values in (9), we get: $\left(\frac{W}{L}\right)_{\mathbf{3,4}} = \mathbf{3.4}$

Choose L = 500 nm$\rightarrow$W = 1.7 μm.

Step 4: Design for M5 from the minimum input voltage [ICMR(-)]

$$\left(\frac{W}{L}\right)_{5,8} = \frac{2I_5}{\mu_n C_{ox}(V_{Dsat})^2} \quad (10)$$

Substituting the values in (10), we get :

$$\left(\frac{W}{L}\right)_{5,8} = \mathbf{0.94}$$

Choose L = 500 nm $\rightarrow$ W = 470 nm.

Step 5: Find M6 from g_{m6} and g_{m4}

$$g_{m6} = 2,2 g_{m1}\left(\frac{C_L}{C_C}\right) = 800\mu A/V$$

$$g_{m4} = \sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right).2I_{D4}} = 73\mu A/V$$

We have :

$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = \frac{I_6}{I_4} = \frac{g_{m6}}{g_{m4}} \Rightarrow \left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{g_{m4}}.\left(\frac{W}{L}\right)_4 = 41$$

Choose L = 200 nm $\rightarrow$ W = 8.2 μm.

Step 6: Caculating of M7 from I_6 and I_4

$$\frac{I_6}{I_4} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} \Rightarrow I_7 = I_6 = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4}.I_4 = 120\mu A$$

We have:

$$\frac{I_7}{I_5} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5} \Rightarrow \left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5}.\left(\frac{W}{L}\right)_5 = 5.64$$

Choose L = 500 nm $\rightarrow$ W = 2.8 μm.
Parameter of M8, we choose the same value of M5.
Calculating parameters of the MOSFET used in the circuit illustrated in Table 3.

Figure 3 shows a schematic diagram of a two-stage CMOS Op-Amp which was designed on Cadence software per the upper procedure. The layout of two stage op-amp using 90nm CMOS technology is illustrated in Fig. 4.

Table 3. Design parameters of two statge Op-Amp

MOSFETS	Aspect ratio (W/L)
M1, M2	6.7
M3, M4	3.4
M5, M8	0.94
M6	41
M7	5.64

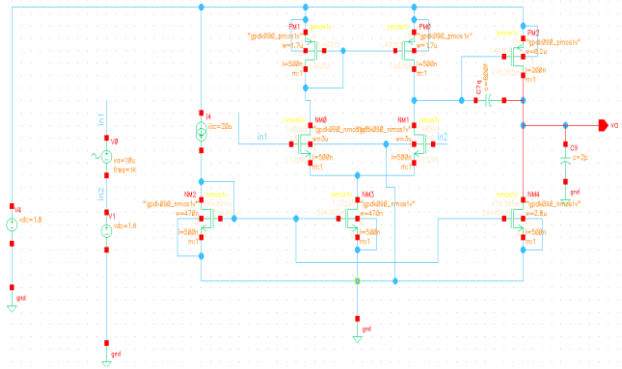

Figure 3. Schematic diagram of two stage CMOS Op-Amp

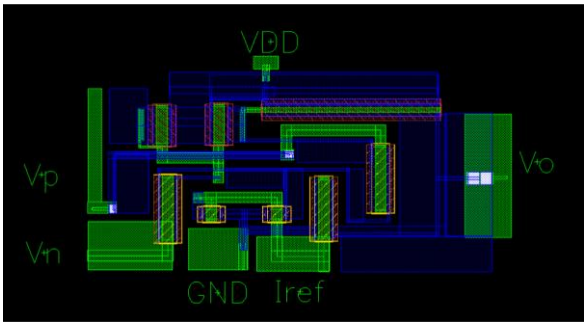

Figure 4. The layout of two stage Op-Amp using 90nm CMOS technology

2.2 Design of single stage Op-Amp

In order to compare the difference between two-stage and single-stage amplifiers, we'll remove one amplifier stage on the planning, the technology and parameters requirements are identical as in table 3, aside from the principle diagram. Schematic diagram of one stage Op-AMP is shown in Figure 5 [11]-[14]. The layout of single stage op-amp using 90nm CMOS technology is illustrated in Figure 6.

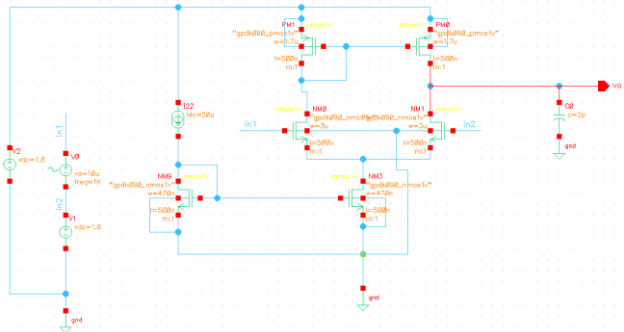

Figure 5. Schematic diagram of single stage CMOS Op-Amp

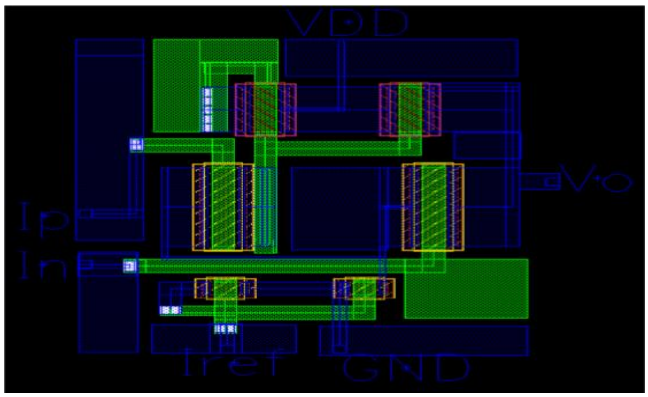

Figure 6. The layout of single stage Op-Amp using 90nm CMOS technology

3. Simulation results and discussion

To check the design with parameters devices as required in Table 3, using AC analysis, we performed simulations of the Gain, Gain Bandwidth, Phase Margin, Slew Rate (SR), and Power consumption.

3.1 With two stage Op-Amp

The gain and gain bandwith, phase margin Slew Rate (SR), and Power consumption were achieved by using AC analysis with designed circuit of two stage Op-Amp and show in Figure 7, Figure 8, Figure 9, and Figure 10 respectively.

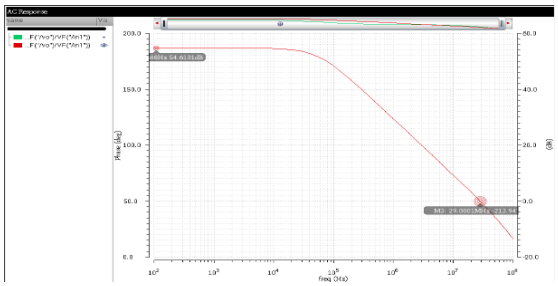

Figure 7. AC analysis representing Gain and Gain Bandwith of two stage Op-Amp

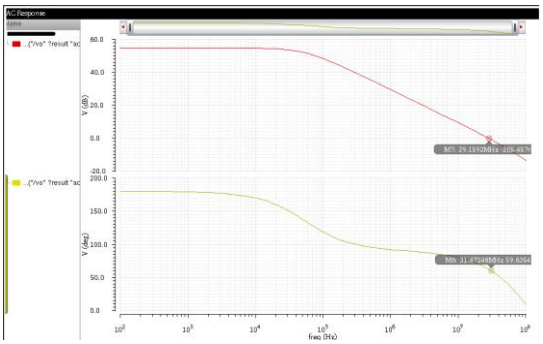

Figure 8. Phase Margin of two stage Op-Amp

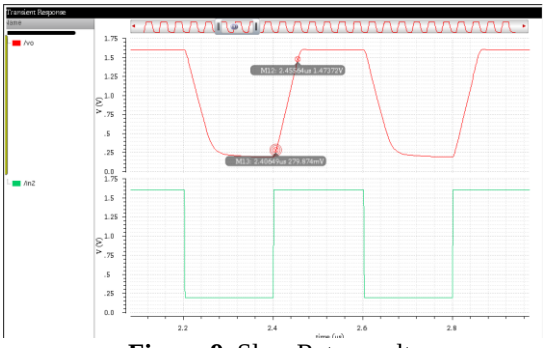

Figure 9. Slew Rate result

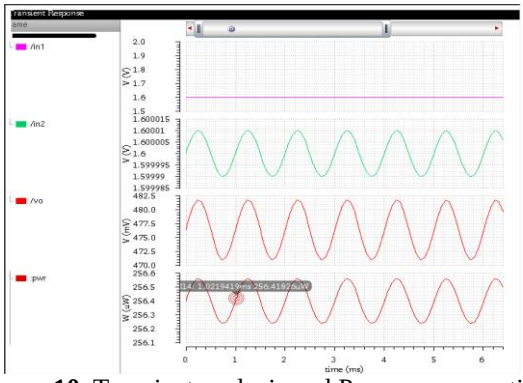

Figure 10. Transient analysis and Power consumption

To get frequency response plot, using an ac signal of 1.5V is swept with 5 points per decade from a frequency of 100Hz to 100MHz.

Figure 7 and Figure 8 illustrate the frequency response of two stage Op-Amp 90nm CMOS technology which shows a dc gain in dB versus frequency in Hz (in log scale) and phase margin of Op-Amp in open loop.

The gain is measured to be 54.6dB and phase margin 120^0 which is fine enough for an Op-Amp operating at a high frequency. A gain of 54.6dB at unity gain frequency of 29MHz and slew rate 24.3V/μs is super for an Op-Amp when all the other parameters also are set at an optimized value.

Slew rate of two stage Op-Amp is calculated using the transient analysis as shown in Figure 9.

Figure 10 shows the transient analysis and Power consumption of two stage Op-Amp using 90nm CMOS technology.

Comparison of parameters for designed circuit with the requirement parameters is given in Table 4.

Table 4. Comparision parameters of two statge Op-Amp

Parameter	Requirement	Simulation
Gain	>50 dB	54.6 dB
Phase Margin	$>60^o$	120^o
Gain Bandwith	30 MHz	29 MHz
Slew Rate	25 V/μs	24.3 V/μs
Power	<=300 μW	256 μW

3.2 With single stage Op-Amp

The gain and gain bandwith, phase margin Slew Rate (SR), and Power consumption were obtained by using AC analysis with designed circuit of single stage Op-Amp and show in Figure 11, Figure 12, Figure 13, and Figure 14 respectively.

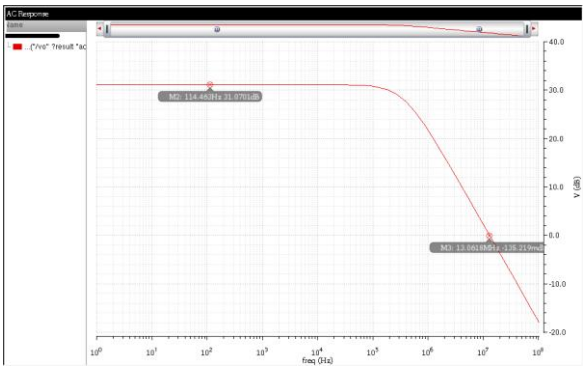

Figure 11. AC analysis representing Gain and Gain Bandwith of single stage Op-Amp

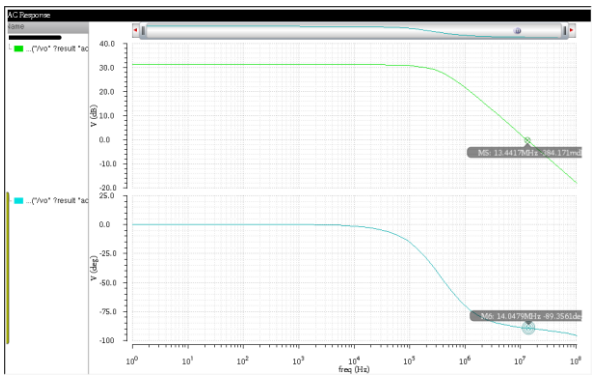

Figure 12. Phase Margin of single stage Op-Amp

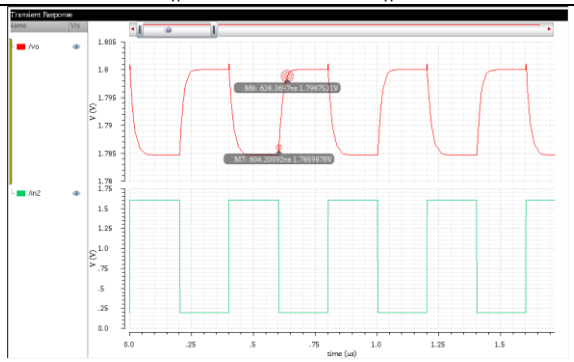

Figure 13. Slew Rate result of single stage Op-Amp

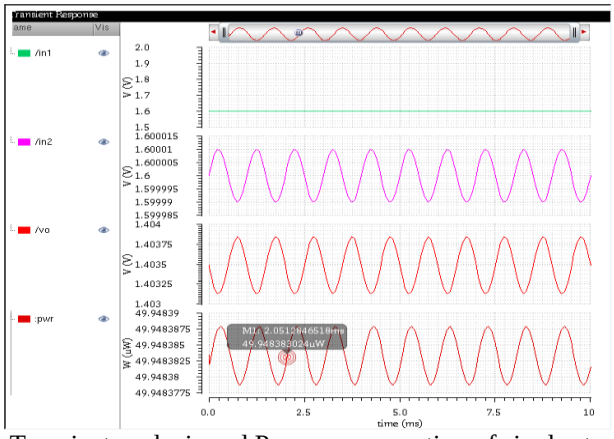

Figure 14. Transient analysis and Power consumption of single stage Op-Amp

Comparison of designing with requirement parameters for single state and two stage Op-Amp is given in Table 5.

Table 5. Parameters comparision

Parameter	Single stage	Two stage
Gain	31.07 dB	54.6 dB
Phase Margin	91^o	120^o
Gain Bandwith	13.06 MHz	29 MHz
Slew Rate	4 V/µs	24.3 V/µs
Power	50 µW	256 µW

From Table 5, we can see the difference in parameters between two configurations of Op-Amp. The parameters of two-stage Op-Amp CMOS circuit almost meets the design requirements, but removing one amplifier stage makes the parameters of design no longer meet the design requirements.

4. Conclusion

In this paper, the authors have proposed design and analysis a two stage and single stage Op-Amp using 90nm CMOS technology, one of the widely used technologies in IC design. In many previous related studies, the authors have hardly shown how to caculate the parameters of the length and width of the MOSFETs.

Two stage and single state Op-Amp circuit are simulated and analyzed in 90nm CMOS technology. Based on the requirements of gain, phase margin, gain bandwith and power consumption to calculate the length and width of the MOSFETs in the circuit. The results show that the power consumption is significantly reduced, suitable for each use purpose. With the single stage Op-Amp circuit, the parameters of design no longer meet the design requirements.

Acknowledgements

The author's team thanks for supporting from the Thai Nguyen University of Technology (TNUT) of Viet Nam for the team to design and complete study.

References

[1] Bộ môn Kỹ thuật Điện tử, Bài giảng Kỹ thuật điện tử tương tự, Khoa Điện tử -Trường Đại học kỹ thuật công nghiệp, 2019.
[2] Nguyễn Hữu Chọng , Nghiên cứu và thiết kế IC Khuếch đại thuật toán sử dụng công nghệ CMOS 130nm, Luận văn Thạc sĩ kỹ thuật Kỹ thuật truyền thông , Đại học Bách Khoa Hà Nội, 2014.
[3] Phillip E. Allen, Douglas R. Holberg, CMOS Analog Circuit Design, 3rd ed., Oxford University Press, pp. 243-341, 2012.
[4] Adel S.Sedra, Kenneth C. Smith, Microelectronic Circuits, 7th Edition, Oxford University Press, 2014.
[5] Ajay Kumar Singh, Electronic Devices And Integrated Circuits, 2nd Edition, PHI Learning Private , Limited, 2013.
[6] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
[7] R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, 3rd Edition, Wiley-IEEE Press, pp. 876-895, 2010.
[8] Behzad Razavi, Design of Analog CMOS Integrated Circuits, Mcgraw-Hill Higher Education, 2001.
[9] Tertulien Ndjountche, CMOS Analog Integrated Circuits High-Speed and Power-Efficient Design, 1st ed., CRC Press, 2011.
[10] Tony Chan Carusone, David Johns, Kenneth Martin, Analog Integrated Circuit Design, 2nd Edition, Wiley, 2011.
[11] Mohd Haidar Hamzah, U. Hashim, Asral Bahari Jambek, Design and Analysis of a Two-stage CMOS Op-amp using Silterra's 0.13 µm, 2014 IEEE Symposium on Computer applications & Industrial Electronics (ISCAIE 2014),Penang, Malaysia, April 7-8, 2014.
[12] Kanika Sharma1, Rahil Kumar, Design of a Two Stage CMOS Operational Amplifier using 180nm and 90nm Technology, IJAREEIE, Vol. 5, Issue 5, pp. 3624-3634, May 2016.
[13] Chirag Mahetaa, Prof.Rakesh Gajareb and Prof.Ankit Adesara, Design and Analysis of Two-Stage CMOS Op-Amp with the Effect of Scaling-Review, International Journal of Innovative and Emerging Research in Engineering (IJIERE), Volume 3, Issue 3, pp. 93-97, 2016.
[14] Anand Kasundra, Jaydip Ravia, Chetan Bhetariya, Himat Chavada, Single Stage and Two Stage OP-AMP Design in 180nm CMOS Technology, IJSTE - International Journal of Science Technology & Engineering,Volume 2, Issue 10, pp. 514-520, April 2016.