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Design and Implementation of a new 4- Bit ALU using Full-Swing Adder with Gate Diffusion Technique (GDI)

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Abstract: In the Electronics Industry, Area and Power dissipation are the main important issues in VLSI Circuits. This paper presents a low power 4-Bit Arithmetic Logic Unit (ALU) using GDI Technique, which considered an effective method for low power and area digital design while reducing the delay and area of VLSI circuits compared to the previous designs. The Proposed ALU is designed by GDI based 2x1 MUX, 4x1 MUX and Full-Swing Full adder to realize arithmetic and logic operations and consume low chip area, less delay and low power consumption than previous design. This Proposed ALU is implemented by using Tanner Tool and Simulation results are carried out by Hspice using 65nm and 32nm with supply voltage 1.2V.

Keywords: GDI, ALU, Full- Swing Full adder, Multiplexers, Logical Functions.

1. Introduction:

In real time applications, ALU is an important component in all electronics, processors and embedded systems. In most of the circuits, power consumption as well as time depends on ALU configurations because all arithmetic and logical operations of circuits are performing in ALU. ALU is also one of the highest power density locations in the processor. The optimization of ALU can be done in three important VLSI parameters which include area, power dissipation and delay. The optimization of ALU for lower power dissipation and faster device performance is of mainly important. Power optimization is possible at every level of digital design flow; however, benefits are more at the architecture design level and transistor level.

In the design of low power digital logic circuits, CMOS is an important element which including microprocessors and ALU within it. Due to the leakage current problem, the static power consumption of CMOS device is almost negligible. However, the addition of the transient power consumption (PT) and capacitive load power consumption (PL) the dynamic power dissipation is used significantly. Mostly this type of dynamic power is dissipated in translating charges in the parasitic capacitors in the CMOS gates.

In VLSI, There are different methods are used to control the power consumption at the architecture device level and module level which includes scaling, varying frequency of operation or supply voltage, changing the load capacitances, etc. Here, in this paper, we are concentrating about optimizing power requirements and delay at the module level.

Power consumption, area and delay are the main important issues in VLSI industry, which triggered many research efforts are tried to minimize the power consumption, area and delay of VLSI circuits. There is only a limited amount of power available for electronic devices heavily used on a daily basis; these devices are low power high speed VLSI circuit works simultaneously. ALU has been a key element used in many applications such as microprocessor, image processing, digital signal processing etc., An essential component of arithmetic unit and almost all other arithmetic operations includes addition therefore any improvement in the adder cell is reflected as a major improvement in the ALU. Hence, the delay also becomes one of the important design parameters which need to be reduced as less as possible.

In ALU, adders play a major role not only in addition but also in performing many other basic arithmetic operations like subtraction, multiplication etc. So many VLSI researchers are designed are several adder designs for optimizing low power requirements, area and delay. Several works have been proposed in the literature for low power ALU design. An ALU is implemented by two main modules: one module is arithmetic unit performing addition/subtraction operations and the other module is Logic unit.

For a low power designs, Gate diffusion input technique is a new design style for reducing area and delay than the existing adders. Several ALU designs are implemented to design various adders even though the Full-Swing design of GDI based ALU shows high power dissipation and delay than a Proposed ALU design. A new ALU is designed with GDI based Logic functions shows low power dissipation, area and delay than Full-Swing GDI based Full adder [1].

In this paper, a new N-Bit ALU is designed using a low power GDI based Logic functions are compared to Full- Swing GDI based adder [1] in terms of power dissipation and transistor count. Simulation environment is Tanner tool using HSpice 65nm and 32nm process with 1.2V supply voltage.

2. GDI overview:

There are more number of techniques are used for reducing the power, delay and area of VLSI circuits. Gate Diffusion Input (GDI) technique is one of the effective methods for reducing low power digital design circuits using less area compared CMOS and Pass Transistor Logic (PTL). GDI Technique was first proposed by Arkadiy Morgenshtein, Idan Shwartz and Alexander Fish [3]. The main advantage of this technique that it maintaining low complexity of the logic design and allows the implementation of many complex logic functions using only two transistors as listed in Table 1, and the figure of GDI cell is shown below. But it was proposed for fabrication in twin-well CMOS or silicon on insulator (SOI) processes and similar to PTL. Due to threshold drops, the GDI gates suffered from reduced voltage swing at their outputs. This increased static power dissipation and caused performance degradation.

To overcome the reduction of voltage swing at their outputs, Morgenshtein et al. [4] proposed a modified GDI cell. In this Mod GDI cell, the substrate of PMOS and NMOS terminals of GDI cell is permanently connected with a VDD and GND. This modification allows fabrication of GDI cell in standard CMOS processes which is cost efficient compared to twin-well and (SOI) processes.

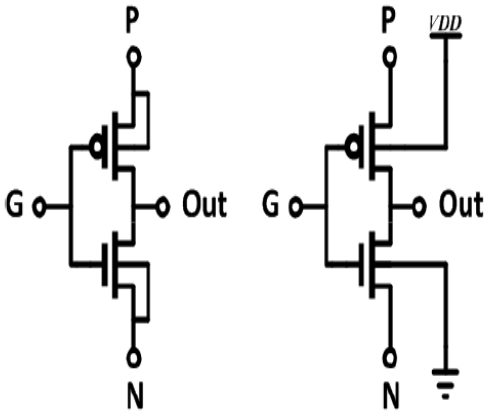

Figure 1: Original GDI cell & Modified GDI Cell

In [5] the proposed Full-Swing GDI cells, swing restoration buffers are used. In this technique, swing restoration transistor utilized to improve the output swing of F1 and F2 gates (universal gates used to realize any logical expression). In this full swing operation, it can be achieved using additional transistors. When compared to CMOS and PTL, this GDI technique uses less number of transistors which leads to reduce the area, power and increasing speed of the circuits. Realization of logic gates is implemented using GDI technique as follows:

Table 1: Realization of different logic functions using GDI cell

N	*P*	*G*	*FUNCTION*	*OUTPUT*
0	1	A	NOT	A bar
0	B	A	F1	A bar B
B	1	A	F2	A bar + B
1	B	A	OR	A + B
B	0	A	AND	AB
C	B	A	MUX	MUX

3. Full Adders:

3.1. Full Swing GDI based Full adder:

The Full adder is mainly improves the overall performance of the VLSI system. In the previous ALU design, the Full adder is implemented by Full swing GDI technique in [1]. This Full adder consumes low power and high speed. It consists of 22 transistors as illustrated in the below Figure 2 and the results are simulated by using HSPICE 65nm & 32nm technology.

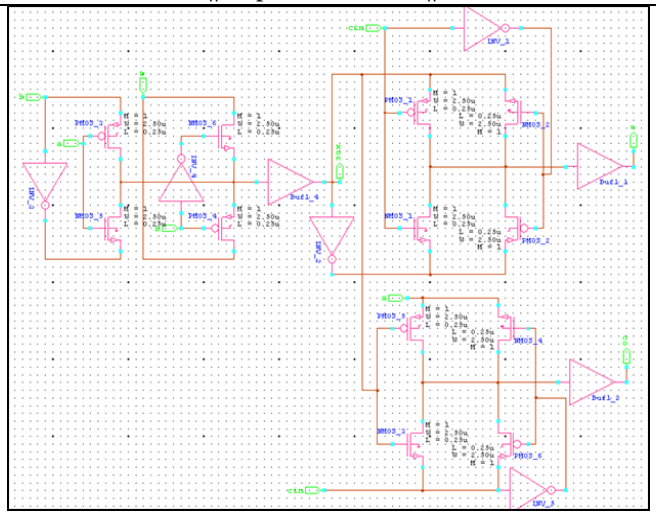

Figure 2: Full-Swing GDI based Full adder

This Full adder is used in both previous Full adder of 1-bit ALU design with 14 transistors Logical block [1] and Proposed Full adder of 1-bit ALU design with 12 transistors Logical block.

3.2. Logical block:

The other block of ALU is logical unit. In this block, full adder is used for arithmetic operations, this adder reduces transistor count but the delay will be very high. In this logical block 12 transistors are used compared to the previous logical block [1], 14 transistors are used and also performing same GDI technique. By reducing delay time, some separate GDI based logic functions are including in this logical block. The main advantage of using this new GDI based logical blocks are reducing transistor count, less power dissipation, less delay and high speed.

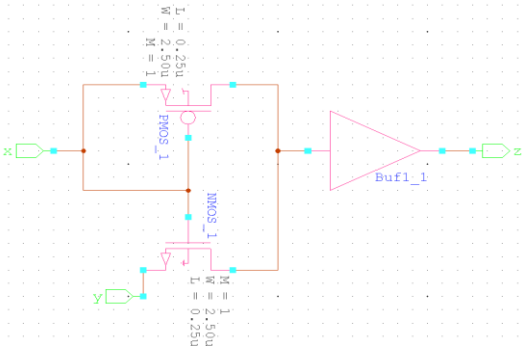

Figure 3: GDI based AND gate

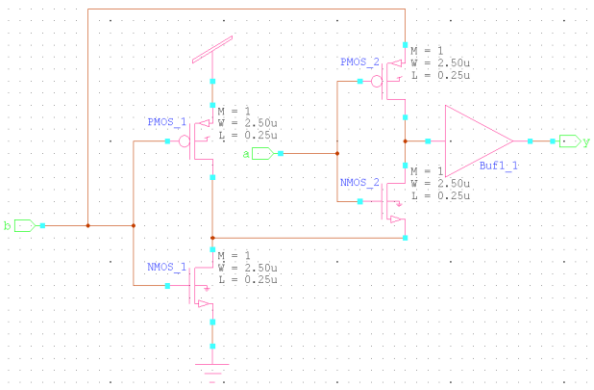

Figure 4: GDI based EXOR gate

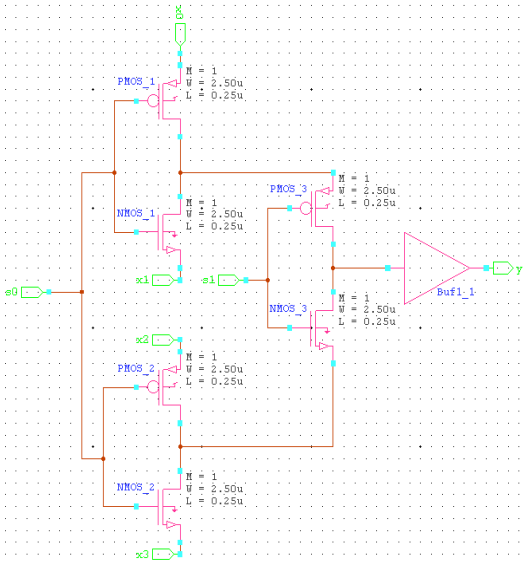

Figure 5: GDI based EX-NOR gate

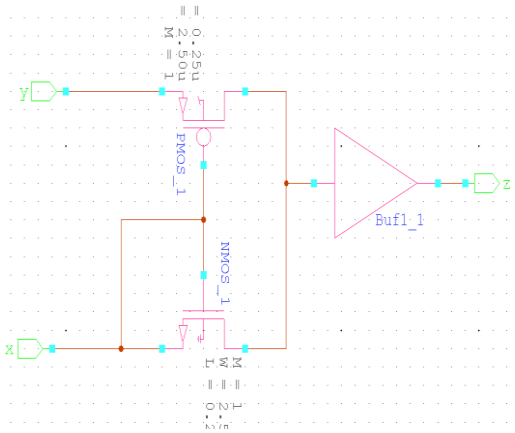

Figure 6: GDI based OR gate

3.3. Multiplexer:

Multiplexer is a combinational circuit that has maximum of 2^n data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines.

Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination will select only one data input. Multiplexer is also called as **Mux**. A Multiplexer circuit acts as a digital switch that selects binary information from one of many input lines and directs the information to a single output line. The selection of a specific input line is controlled by a set of selection inputs.

The implementation of 2x1 and 4x1 multiplexers are designed by using GDI technique as illustrated in Figure 7 and Figure 8 respectively. In this 2x1 multiplexer is constructed by 2 transistors and 4x1 multiplexer also constructed by 6 transistors because these multiplexers are designed by using GDI technique as illustrated.

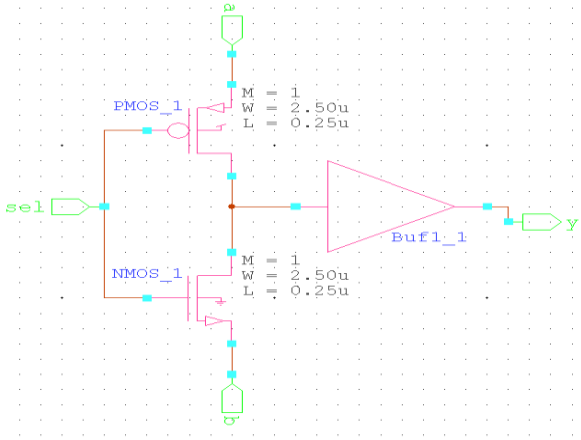

Figure 7: GDI based 2x1 MUX

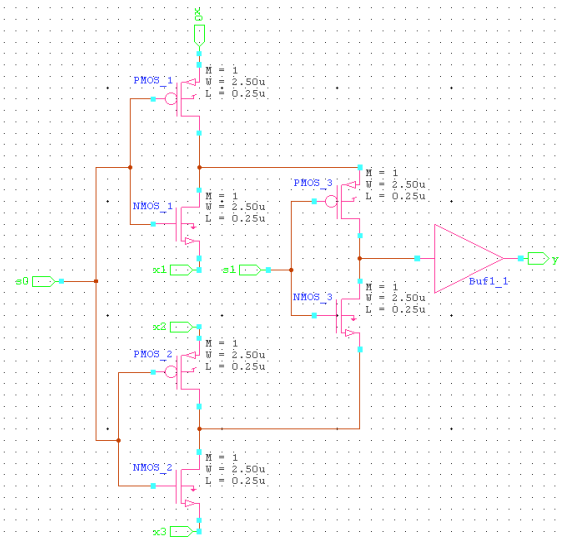

Figure 8: GDI based 4x1 MUX

In these Multiplexers, new GDI based 2x1 MUX and 4x1 MUX are compared to Previous Design [1] of 2x1 and 4x1 Multiplexers.

4. ALU:

An **Arithmetic Logic Unit** (**ALU**) is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers. This is in contrast to a floating-point unit (FPU), which operates on floating point numbers. An ALU is a fundamental building block of many types of computing circuits, including the central processing unit (CPU) of computers, FPUs, and graphics processing units (GPUs). A single CPU, FPU or GPU may contain multiple ALUs.

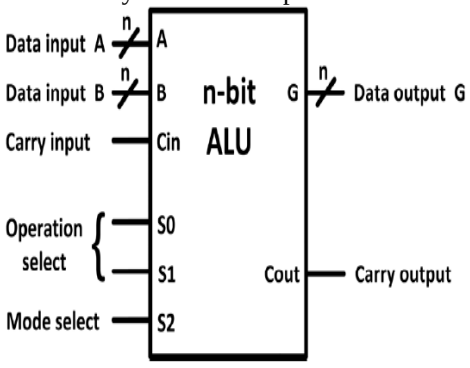

Figure 9: Block diagram of N- bit ALU

The above Figure 9 shows the block diagram of N- bit ALU performing both arithmetic and logic operations. It has three selection inputs such as S0, S1 and S2 performs between arithmetic and logic operations. It has n data inputs and outputs (A & B) and one carry input (Cin) to generate operation of data output G and one Carry output (Cout).

ALU design is proposed by M. A. Ahmed and M. A. Abdelghany, which optimized to reduce delay time using different full adder and a separate logic block to perform the logical functions while maintaining low power operation and full-swing output. The Proposed 1-bit ALU is designed as shown in Figure 10 by Full adder, new GDI based logic block, 4x1 Multiplexer, 2x1 multiplexer and Inverter.

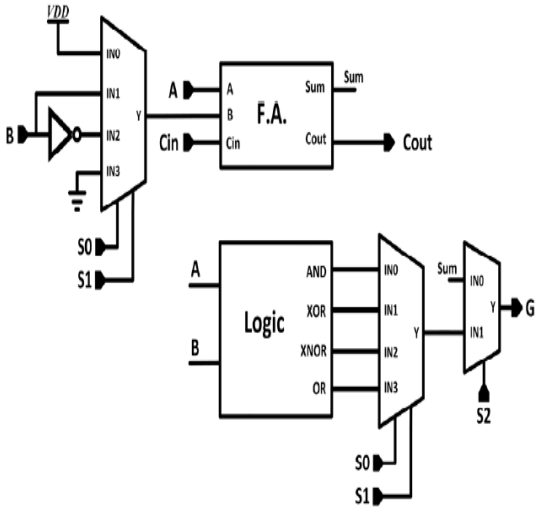

Figure 10: Proposed diagram of 1- bit ALU

In this proposed 1-bit ALU design, 4x1 multiplexer consists four inputs VDD, B, B bar, ground, two selection inputs S0 and S1 as 2-bit binary information and one output Y. the 4x1 multiplexer output Y is connected to one of the input of Full- Swing GDI based Full adder and other two inputs are A, Cin, it generates two outputs as Sum and Cout. The logical block contains two inputs A, B and generate four logical output functions like AND, XOR, XNOR, OR i.e., four outputs. These four outputs are taken as inputs of 4x1 multiplexer with two selection inputs S0, S1 and generate one output Y. the 4x1 Multiplexer output Y is connected to one of the input of 2x1 Multiplexer input and other input is one of the Full adder output as Sum with selection input S2 and generate ALU output as G.

$$G = A + B + Cin$$

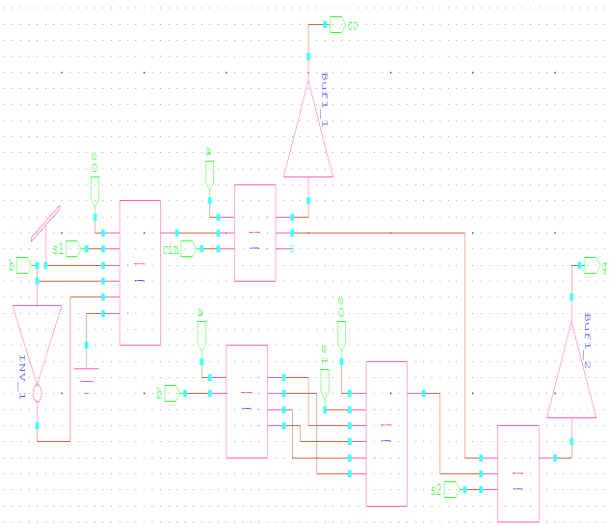

Figure 11: Implementation of 1- bit ALU using Tanner Tool

The above Proposed 1-bit ALU design is implemented completely with low transistor count(50) of 4x1 MUX(6), Full-Swing GDI based Full adder(22), Logical block(12), 2x1 MUX(2), INV(2) compared to the previous design of 1-bit ALU [1] is implemented with transistor count(72) of 4x1 MUX(16), XNOR based Full adder(18), Logical block(14), 2x1 MUX(6), INV(2).

Table 2: Functional Truth table of 1-bit ALU

S0	*S1*	*S2*	*Operations*	*Function*
0	0	0	G = A - 1	DECREMENT
1	0	0	G = A + B	ADDITION
0	1	0	G = A + B bar + 1	SUBTRACTION
1	1	0	G = A + 1	INCREMENT
0	0	1	G = A ^ B	AND
1	0	1	G = A XOR B	EXOR
0	1	1	G = A bar	EXNOR
1	1	1	G = A ν B	OR

For decrement operation, A is summed with logic 1 which represents -1 in 2's complement with Cin = 0, then the output G = A – 1. In addition operation, A is summed with B with Cin = 0, then the output G = A + B. Subtraction is achieved using 2's complement A is summed with the complement of B with Cin = 1, then the output G = A +B + 1 which equivalent to A – B. And for increment operation A is summed with logic 0 with Cin = 1, then the output G = A + 1.

According to S0 and S1, the second 4x1 multiplexer used for selection of logic operation. While the second 2x1 multiplexer used to selects between arithmetic and Logic operation.

5. Implementation of N-bit ALU:

In this N-bit ALU's, GDI based logic functions (12T), Full adder (18), 2x1 MUX (2T), 4x1 MUX (6T) are used for reducing the Chip Area, Low Power, less Delay and High Speed performance.

The 4-bit and 8-bit ALU's are implemented by using 1-bit ALU design by Tanner Tool with HSPICE using 65nm & 32nm Technology.

5.1. 4-bit ALU:

This 4- bit ALU is implemented by cascading connection of Four stages of 1-bit ALU and one 2x1 multiplexer as shown below Figure 12. It consists of a0 to a3 and b0 to b3 inputs and carry input as c0 and three selection inputs s0, s1 and s2 and generate outputs G0 to G3 and one carry output.

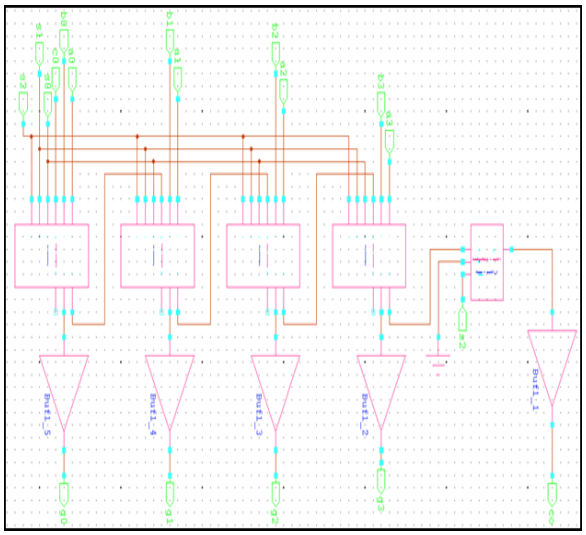

Figure 12: Implementation of 4- bit ALU

5.2. 8-bit ALU:

This 8- bit ALU is implemented by cascading connection of Two stages of 4-bit ALU and one 2x1 multiplexer as shown below Figure 13. It consists of a0 to a7 and b0 to b7 inputs and carry input as c0 and three selection inputs s0, s1 and s2 and generate outputs G0 to G7 and one carry output.

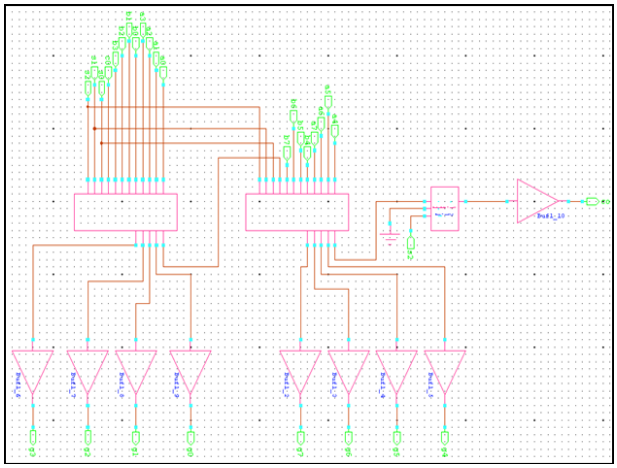

Figure 13: Implementation of 8- bit ALU

6. Simulation Results:

The proposed 4-Bit and 8-Bit ALU designed using 65nm & 32nm Tanner Tool, The simulations were done using the HSPICE with a power supply 1.2V, for best power and delay performance. The Proposed design is compared to the previous design [5] in terms of power consumption, delay, energy and transistor count. Simulation results for the Proposed 4-bit and 8-bit ALU are shown in Table 3.

Table 3: Functional Truth table of 1-bit ALU

Full adder	N -Bit ALU	Transistor Count	65nm		32nm	
			1.2V		1.2V	
			Delay (Sec)	Power dissipation (watts)	Delay (Sec)	Power dissipation (watts)
Previous Design [1]	4-Bit	294	1.61e^-8	2.98e^-4	1.60e^-8	1.90e^-4
	8-Bit	590	1.64e^-8	6.43e^-4	1.61e^-8	4.09e^-4
Proposed Design	4-Bit	202	1.61e^-8	2.21e^-4	1.60e^-8	1.71e^-4
	8-Bit	406	1.63e^-8	4.82e^-3	1.61e^-8	3.67e^-4

7. Conclusion:

In this paper, delay time of a 4-Bit and 8-Bit ALU designed using the Full-Swing based Full adder is optimized and reduced by 20% compared to the previous design, while maintaining full-swing operation. The Proposed 1-bit ALU design consists of **50** transistors and operates under 1.2V supply voltage, based on the results, it can be concluded that the proposed 4-bit ALU is suitable for low energy high-speed VLSI applications. Further study in this work would be using the 8-bit ALU as a building block to implement 16-bit and 32-bit ALU.

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