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Control of VC IIDG and PQ-IIDG for Microgrid under Different Fault Conditions

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Abstract: In this paper, the modeling of a micro grid is presented. Developed fault models of IIDGs and voltage-controlled IIDGs. Considering that the control strategy of the PQ-controlled IIDG varies, to reflect its fault characteristics as comprehensive as possible Voltage-controlled IIDG is of great significance on maintaining a stable microgrid. The model of voltage-controlled IIDG proposed in this paper keeps its voltage-source nature while accomplishing current limiting. The performance of the proposed IIDG fault models has been implemented in Matlab Simulink environment and the results are presented.

I. Introduction

Current utility practices do not permit autonomous micro-grid operation and, except in special cases, require that all downstream DG units be disconnected after either planned or unplanned switching events. This requirement is imposed to address safety concerns and to comply with the existing control/protection constraints of distribution systems [3], [4]. However, to realize the full benefit of high DG penetration depth, the autonomous operation of micro-grids needs to be considered.

II. Micro Grids on the Distribution System

Every distribution utility has an obligation to supply its customer's electricity at a voltage within a specified limit. This requirement often determines the design and expense of the distribution circuit so that over the years techniques have been developed to make the maximum use of distribution circuits to supply customers within the required voltage [1]. Some distribution utilities use more sophisticated control of the on load tap changers of the distribution transformer by regulators on the feeder and including the use of the current signal compounded with the voltage measurement at the switched capacitor on feeders [9]. Feeding power from a Distribution Generator (DG) unit can cause negative impacts on the network voltage in case a DG unit is placed just downstream to a load tap-changer transformer [10]. In this case, the regulators will not correctly measure the feeder demands. Rather, they will see lower values since the DG unit reduces the observed load due to the onsite power generation. This will lead to setting the voltage at lower values than that required to maintain adequate levels at the tail ends of the feeder [10]. However, the most favorable locations of DG units near the end user terminals can provide the required voltage support at the feeder nodes.

III. Fault Analysis

Electrical networks and machines are subject to various types of faults while in operation. During the fault period, the current flowing is determined by the internal e.m.f of the machines in the network, and by the impedances of the network and machines. However, the impedances of machines may change their values from those that exist immediately after the fault occurrence to different values during the fault till the fault is cleared. The network impedance may also change, if the fault is cleared by switching operations. It is, therefore, necessary to calculate the short-circuit current at different instants when faults occur. For such fault analysis studies and in general for power system analysis it is very convenient to use per unit system and percentage values.

In the analysis of symmetrical three-phase short circuits the following assumptions are generally made. Transformers are represented by their leakage reactance. The magnetizing current, and core fusses are neglected. Resistances, shunt admittances are not considered. Star-delta phase shifts are also neglected. Transmission lines are represented by series reactance. Resistances and shunt admittances are neglected. Synchronous machines are represented by constant voltage sources behind sub transient reactance. Armature resistances, saliency and saturation are neglected. All non-rotating impedance loads are neglected. Induction motors are represented just as synchronous machines with constant voltage source behind a reactance. Smaller motor loads are generally neglected.

Faults kill. Faults start fires. Faults force interruptions. Faults create voltage sags. Tree trimming, surge arresters, animal guards, cable replacements: these tools reduce faults. We cannot eliminate all faults, but appropriate standards and maintenance practices help in the battle. When faults occur, we have ways to reduce their impacts. This chapter focuses on the general characteristics of faults and specific analysis of common fault types with suggestions on how to reduce them. One of the definitions of a fault is (ANSI/IEEE Std. 100-1992):

Fault: A physical condition that causes a device, a component, or an element to fail to perform in a required manner; for example, a short circuit or a broken wire. A fault almost always involves a short circuit between energized phase conductors or between a phase and ground. A fault may be a bolted connection or may have some impedance in the fault connection. The term "fault" is often used synonymously with the term "short circuit" defined as (ANSI/IEEE Std. 100-1992):

Short circuit: An abnormal connection (including an arc) of relatively low impedance, whether made accidentally or intentionally, between two points of different potential. (*Note:* The term *fault* or *short-circuit fault* is used to describe a short circuit.)

When a short-circuit fault occurs, the fault path explodes in an intense arc. Local customers endure an interruption, and customers farther away, voltage sag; faults cause most reliability and power quality problems. Faults kill and injure line operators. The maximum currents occur with a bolted fault, where R_F is zero. The maximum current for a line-to-line fault is 86.6% of the maximum three-phase fault current. In all cases, the load current is ignored. In most cases, load will not significantly change results. The three-phase fault current is almost always the highest magnitude. On most circuits, the zero-sequence impedance is significantly higher than the positive-sequence impedance.

IV. Electrical Power Quality

Electrical power quality is one of the most modern branches in power system study. Electric Power Quality (EPQ) is a term that refers to maintaining the near sinusoidal waveform of power distribution bus voltages and currents at rated magnitude and frequency. This chapter describes in brief the causes of poor power quality in power system. Need of research on electric power quality is highlighted. This chapter also highlights the power system disturbances related to rise or fall of rms voltage. Then it describes these disturbances one after another along with their main causes and effects.

The sources of poor power quality can be categorized in two groups: (1) actual loads, equipment and components and (2) subsystems of transmission and distribution systems. Poor quality is normally caused by power line disturbances such as impulses, notches, voltage sag and swell, voltage and current unbalances, momentary interruption and harmonic distortions. The International Electro-technical Commission (IEC) classification of power quality includes loss-of-balance as a source of disturbance. IEEE standard also includes this feature as a source of quality deterioration of electric power. The other major contributors to poor power quality are harmonics and reactive power. Solid state control of ac power using high speed switches are the main source of harmonics whereas different non-linear loads contribute to excessive drawl of reactive power from supply. It leads to catastrophic consequences such as long production downtimes, mal-function of devices and shortened equipment life.

V. Simulation Result Analysis

In this section, simulation results are presented for events include line outage and three-phase short circuit fault.

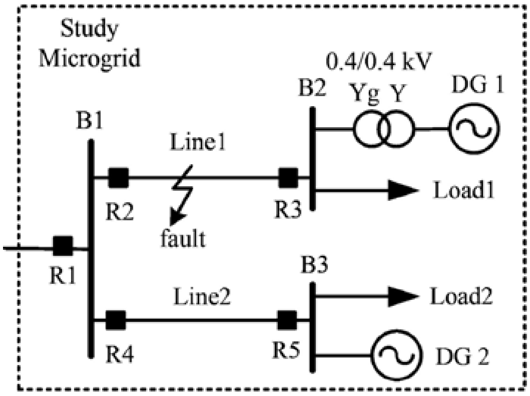


Fig.1: micro-gird

In this paper developed the fault model concepts using Matlab Simulink. The fault models of PQ-IIDG and V/f-IIDG were tested in a 0.4 kV microgrid as shown in Fig.1.

Case 1: Single Phase Fault

At 0.08 s, phase 'A' ground fault occurs at the Line1and the fault resistance is 1 Ω. The simulation results of DG1 are shown in Fig.2.

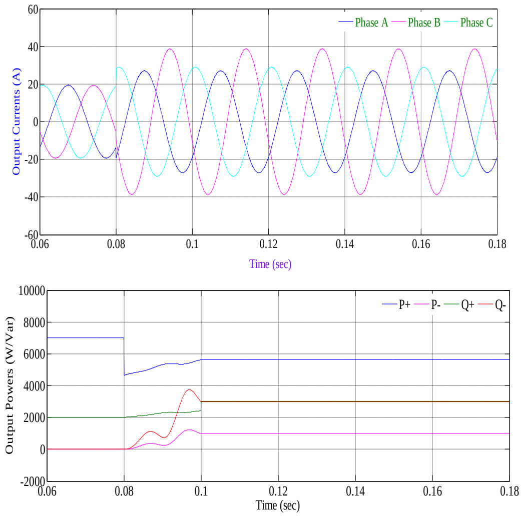


Fig.2: Simulation results of DG1

The simulation results of DG2 are shown in Fig. 3. Because the peak current of phase A is limited to 80 A, the post-fault voltage of phase 'A' drops to about 64 V. The reason is that the fault response of PQ-IIDG influences the equivalent impedances of V/f-IIDG's healthy phases, thus the currents of phase B and C are different with the corresponding pre-fault currents.

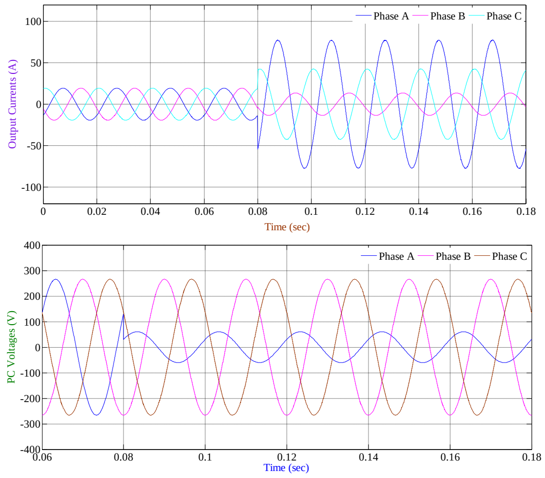
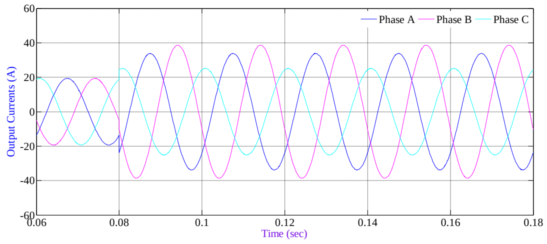


Fig.3: Simulation results of DG2

Case 1: Two-Phase Fault



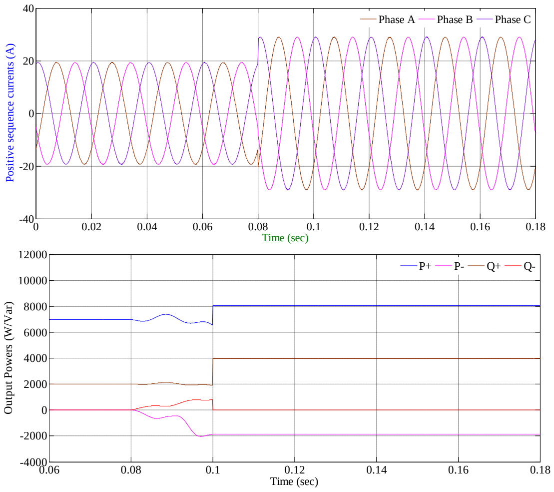


Fig.4: Simulation results of DG1

At 0.08 s, short circuit fault between phase A and phase B occurs at the Line1 and the fault resistance is 2 Ω. The simulation results of DG1 are shown in Fig. 4. The peak value of positive sequence current is 30 A. The simulation results of DG2 are shown in Fig.5. The post-fault voltages of phase A and phase B drop to about 89 V.

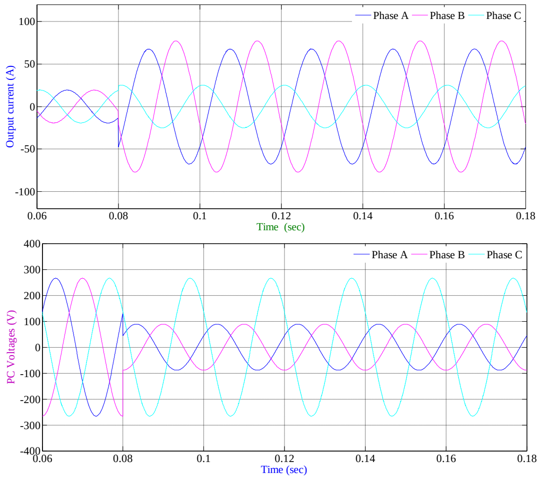
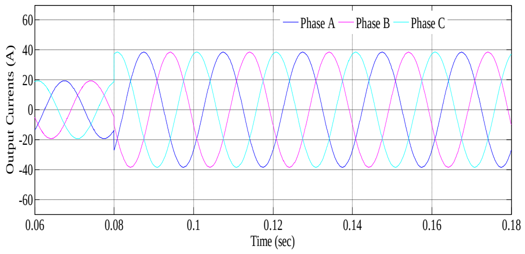


Fig.5: Simulation results of DG2

Case 3: Three-Phase Fault

At 0.08 s, three-phase short circuit fault occurs at the midpoint of Line1. The fault resistance is 2 Ω. The simulation results of DG1 are shown in Fig. 6. The total supplied active power and reactive power are 3.94 kW and 6 kvar. The reactive power has a higher priority, so the active power is reduced to achieve current limiting in this case. The simulation results of DG2 are shown in Fig.7. The post-fault three phase voltages drop to 68 V.



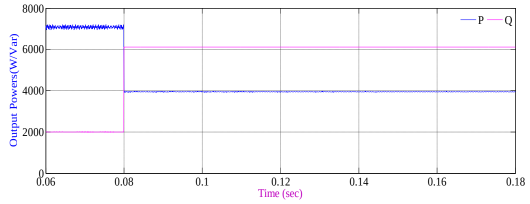


Fig.6: Simulation results of DG1

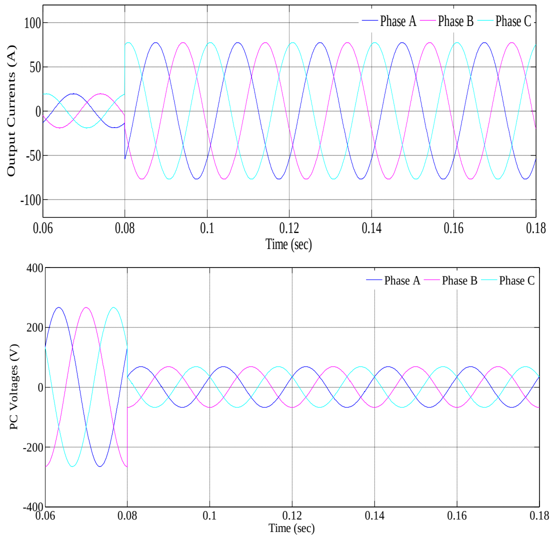


Fig.7: Simulation results of DG2

VI. Conclusion

In this paper, the Microgrid System in Grid-Connected Mode and Islanding mode is analyzed. The modeling of microgrid system is developed in Matlab Simulink environment and simulation results are discussed and presented.

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