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Implementation of BPSK Modulator on FPGA

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Abstract: This paper presents Field Programmable Gate Array (FPGA) implementation of Binary Phase Shift Keying (BPSK) modulation technique.BPSK is the one of the most important methods of digital communication systems, which obtained by the modulating the phase of the binary-pam to the RF (radio frequency) carrier. The modulator includes user controllable input and modulated signal. Numerically Controlled Oscillator that is also called as Direct Digital Synthesizer (DDS), controls the phase of the carrier signalsynchronously and discrete amplitude modulationcreatemodulated waveform with digital to analog converter (DAC) at the output. The present paper improves a solution for implementing the modulation technique on Spartan 3E Starter Kit with VHDL language.

Keywords: BPSK, FPGA, modulation, VHDL, NCO, DDS.

1. Introduction

In the last years, it become necessity to transition from analog to digital modulation techniques in developing communication systems. Digital communication system is more reliable than an analog in terms of signal processing algorithms.It is needed for analog systems excessive number of waveforms and large bandwidth for the symbol transmission operations. Such analogue circuits face heating, high power dissipation and cost problems. However, digital systems can reduce hardware, noise andminimize intersymbolinterference (ISI) problems with high speed and decimated silicon area cost [1].Also, it provides higher data security, best quality communication with large bandwidth and more information capacity. So, instead of analogue circuitry, digital hardware, especially Field Programmable Gate Arrays (FPGAs) are preferred due to their high flexibility and attractive speeds.

Digital modulation is the process, which makes in compatible digital symbol waveforms to form of the channel.The message issent digitally from the source for accepting encoder. The source encoder accepts the digital data and map the input symbols into an output symbols. The binary information is obtained at the output of the channel encoder and is passed to a digital modulator.Then, modulator translate the discrete symbols into an analog waveform that can be transmitted over the channel.

Generally, modulation techniques are known as M-ary modulation. In a M-ary modulation, M bits are used together to form waveforms, and one of the possible waveform obtained is transmitted. M have 2^n number of possibilities, where n isan integer. Depending on the amplitude, phase or frequency, the modulation is implied as M-ary ASK, M-ary PSK or M-ary FSK. In modern communication systems, simply and widely used one is binary modulation (M=2).Most of the research are focused on three basicbinary modulation techniques like BASK (Binary Amplitude Shift Keying), BFSK (Binary Frequency Shift Keying) and BPSK (Binary Phase Shift Keying) [2],[3].Several papers existed in terms of implementing BPSK using FPGA [4]-[7].

2. BPSK Modulator

BPSK is the simplest form of phase shift keying (PSK). It uses two phases of carrier with same frequency but separately by 180^0 can also be determined 2-PSK. Numerically Controlled Oscillator (NCO) generates carrier sinusoidal signal with frequency $f_c$to be mixed with binary signal to produces BPSK signal. Ifthe input bit value "1" is transmitted the modulated signal remain same and if "0" is transmitted signal will change with 180^0 .Transmitted BPSK waveform that producedbybinary signal is multiplied with carrier signal is shown in Figure 1.

If m(t) is called as binary sequence of bipolar format, $f_c$is the frequency of the carrier signal and s(t) is modulated signal, BPSK modulation can be shown as:

$$S(t) = A\sin(2\pi fct) \text{ if } m(t) = 1$$
$$S(t) = -A\sin(2\pi fct) \text{ if } m(t) = 0$$

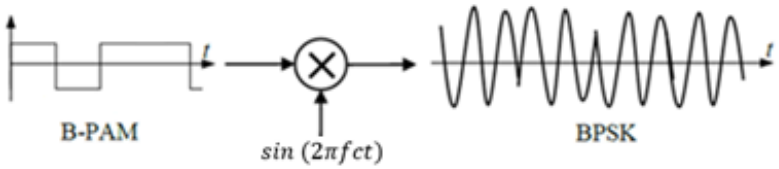

Figure 1:BPSK Modulation

The BPSK modulator Simulink model in Figure 2. consist of two sine carriers, one of them isthe delayed sine values with 180º. Switch will choose between the sine or -sinevalues depending on the pulse generator input. Figure 3. shows the BPSK waveform generated by the corresponding Simulink blockset.

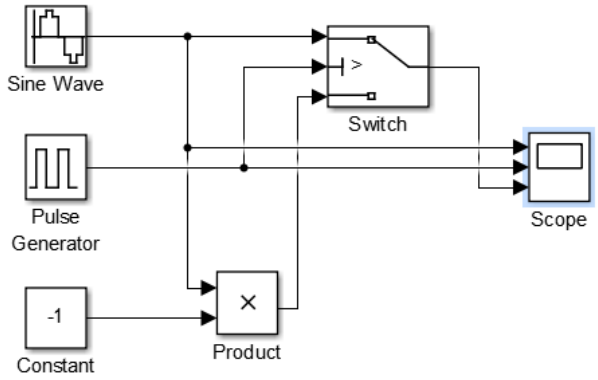

Figure 2: Simulink Model ofBPSK Modulation

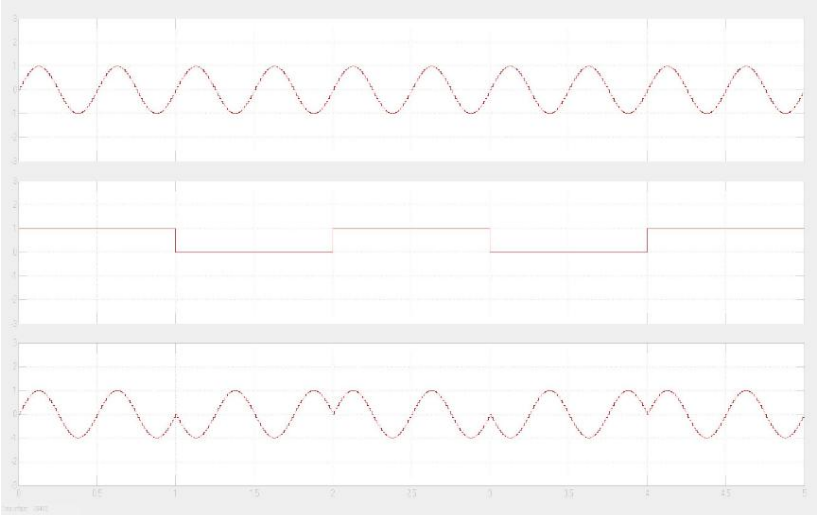

Figure 3: The Scope Output of Waveform

3. FPGA Implementation

This paper does not only present the theoretical designof BPSK modulation, but also implementation of Numerically Controlled Oscillator and DAC module, which is the component of the BPSK modulation. NCOs are commonly used in digital systems, where they used to generate sinusoidal waveforms. In many implementations, NCO is named as Direct Digital Synthesis(DDS). In this work, implementation of Look-up Table based NCO is presented. NCO includes a phase accumulator,some output bits of which drive address input of a ROM filled with samples of a sinusoidal as shown in Figure 4. The ROM stores the K-depth sine values determined by the following equation:

$$\sin\left(\frac{2\pi n}{K}\right),\ n = 0,1,2,\ldots.K-1$$

The number of per cycle of sine sequences is set to K=32, where the value of B_K is taken as 8-bit.

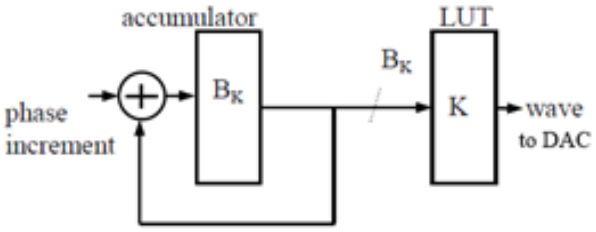

Figure 4: LUT Based NCO

NCO tables or RAM contents can be changed flexibly with a user controllable switch during the operation. When switch is "1" the values are given to the output without no sign changing, otherwise (switch is "0") the sinusoidal waveform changes with 180^0 . This output, which is generated by NCO is send via connection of the FPGA with SPI bus interface into Digital-to-Analog Converterforobservingreal-time resultfromoscilloscope.The Spartan 3E board includes a Serial-Peripheral-Interface (SPI) compatible, DAC and the linear technology LTC2624 device has 12-bit resolution with four outputs. The SPI is a synchronous full-duplex character-oriented bus, which employs five communication wires. The connection of the FPGA with the SPI bus interface and the DAC is shown in the Figure 5[8]. The DAC interface has three inputs like *reset, clock* and *data* and four SPI bus wires (*spi_mosi, spi_sck, dac_cs, dac_clr*). To get the analog signal from one of the four channels, it should be design this interface with DAC using VHDL.

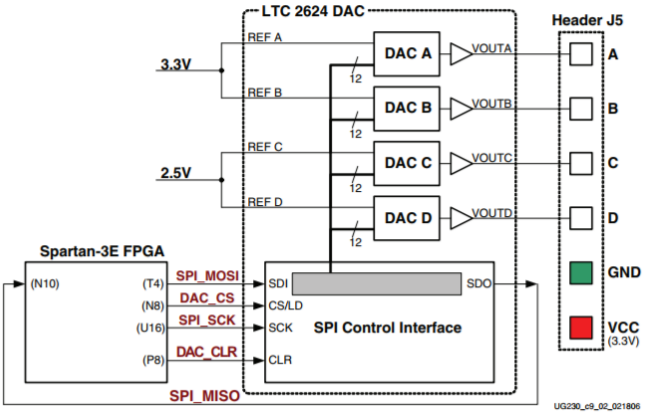

Figure 5:DAC connection Schematic

4. Experimental Results

Implementation specific parameters are obtained using the Xilinx ISE software. The design had a maximum operating frequency of 225.319 Mhz. In Mali, A. S., and Sandeep D. Hanwate work, operating frequency can reach only 113.343Mhz[9]. It has low operating frequency, because they use the using Xilinx System Generator for their study. System generator also requires high number of slices. In this work VHDL is used for all implementations. The logic source usage in terms of slices and multipliers and performance analysis of the architecture were detailed. Design summary results and advanced HDL synthesis report are presented in Figure 6.

The experimental results were carried out in a laboratory using the Spartan 3E FPGA board and a digital oscilloscope, illustrated in Figure 7 while the input binary sequence was controlled by theswitch on the board.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	60	9,312	1%
Number of 4 input LUTs	82	9,312	1%
Number of occupied Slices	60	4,656	1%
Number of Slices containing only related logic	60	60	100%
Number of Slices containing unrelated logic	0	60	0%
Total Number of 4 input LUTs	90	9,312	1%
Number used as logic	82		
Number used as a route-thru	8		
Number of bonded IOBs	14	232	6%
Number of BUFGMUXs	2	24	8%
Average Fanout of Non-Clock Nets	3.39		

Figure 6: Design Summary of the BPSK Modulator

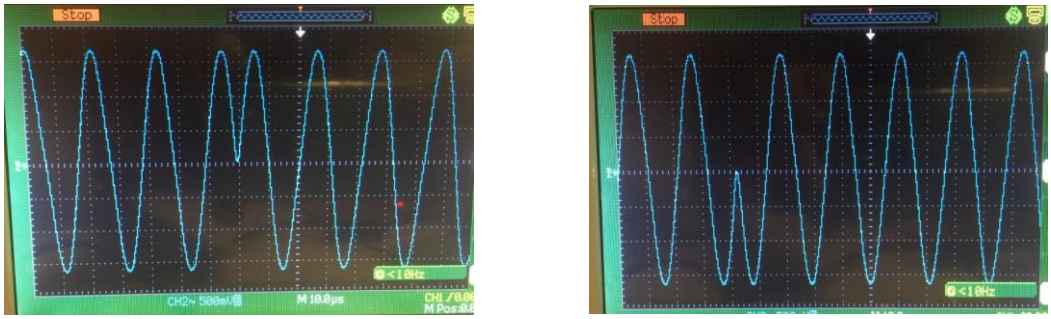

Figure 7: Scope Outputs of Modulated BPSK Waveform

5. Conclusion

Digital modulation is more reliable than analogue modulation in many terms. The FPGA implementation of BPSK digital modulation technique using NCO and DAC modulesare proposed.All of themwere implemented on the Spartan 3E FPGA kit. This provides the parallel implementation of hardware results in faster algorithm execution.Hence, design and implementation results show that, BPSK modulation is well-fitted to FPGA implementation.

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